EIGHTH QUARTERLY SUMMARY REPORT

R & D PROGRAM TO DESIGN AND FABRICATE DIGITAL MONOLITHIC MICROCIRCUITS HAVING AVERAGE PROPAGATION DELAY TIME OF 1 NS

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS AND TABLES

SECTION 1 - INTRODUCTION

1.1 Scope of Report

This report describes the program effort performed under M.I.T. Lincoln Laboratory Subcontract No. 295 (Prime Contract No. AF 19(628)-5167 for the period July 1, 1965 to June 23, 1966. Titled the Eighth Quarterly Summary Report, it summarizes the work performed during the first three quarters of this period, in addition to describing the work performed in the last quarter.

1.2 Program Objectives

This research and development program, had as its primary objective the fabrication of silicon monolithic microcircuits with average propagation delay times in the nanosecond region. This goal was achieved early in the program; as a consequence experiments for the remainder of the program were directed toward achieving subnanosecond microcircuits. A second objective during the latter half of the program was to make preliminary investigation of the technological problems that relate to the fabrication of ultrahigh-speed complex bipolar arrays. The array investigation, which will be continued during a program extension, is directed toward determining the improvements in speed that will be obtained in digital systems through the fabrication and interconnection of many very high speed monolithic circuits within a single chip.

Accepted for the Air Force
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1.3 Areas of Investigation

The achievement of subnanosecond digital microcircuit performance requires a microcircuit structure which features very high speed, high performance transistors and minimal parasitic capacitances. A number of other factors ultimately enter into the determination of microcircuit speeds but, in general, the major requirement for achieving the highest microcircuit speeds is the utilization of the highest performance transistors.

The design principles and the technologies leading to the fabrication of small geometry (0.1 mil), high performance discrete transistors had been developed, in part, during an earlier period (July 1, 1964 to June 30, 1965) of the program. The adaptation of these special small geometry, high performance transistor fabrication techniques to the fabrication of small geometry microcircuits containing high performance transistors constituted the basic approach to obtaining subnanosecond microcircuit performance on this program. In support of the microcircuit effort, development work was continued on transistors with more optimum performance characteristics. Included in the transistor effort was the design and fabrication of a 0.05-mil geometry npn transistor.

The microcircuits which served as the test vehicles for obtaining subnanosecond performance were of the saturated and the

unsaturated variety. The saturated microcircuit was a simple TTL 3-input gate designated SMX1. The unsaturated circuits were two different designs of a basic 3-input ECL gate designated SMX2 and SMX4.

Since digital microcircuit applications often involve the use of large numbers of microcircuits, power dissipation becomes an important consideration. An important part of this program was the study of the speed-power properties and trade-offs in high performance digital microcircuits as they are affected by transistor and circuit design.

During the past two quarterly periods a preliminary study was begun of the problems associated with the design, fabrication, and test of very high speed, high density, single-chip microcircuit arrays. It became apparent as discrete microcircuit speeds substantially less than 1 ns were being obtained, that circuit speeds were becoming increasingly limited by time delays associated with interstage conventional wiring and capacitive loading of individual packaged microcircuits. The array investigation is directed toward predicting the improvements in speed that will be obtained in high speed digital systems by minimizing package-related delays through fabrication of many very high speed monolithic circuits within a single chip.

The vehicles selected for this study were 3-bit, 9-bit and 27-bit ECL versions of a parity generator, containing 58, 232 and

754 components (40, 160, 520 transistors), respectively. These vehicles were selected because they would present all the problems related to designing, fabricating and testing small geometry (0.1 mil), high speed, high density microcircuit arrays. The choice of vehicles was also strongly influenced by results of the speed-power studies indicated above.

Finally, a developmental ECL computer circuit being evaluated by Lincoln Laboratory in discrete component form was designed and fabricated in microcircuit form (SMX3). The purpose of this effort was to optimize the speed performance of an existing circuit design, where dc operating levels were already defined, by the application of high speed, high performance microcircuit design and fabrication techniques.

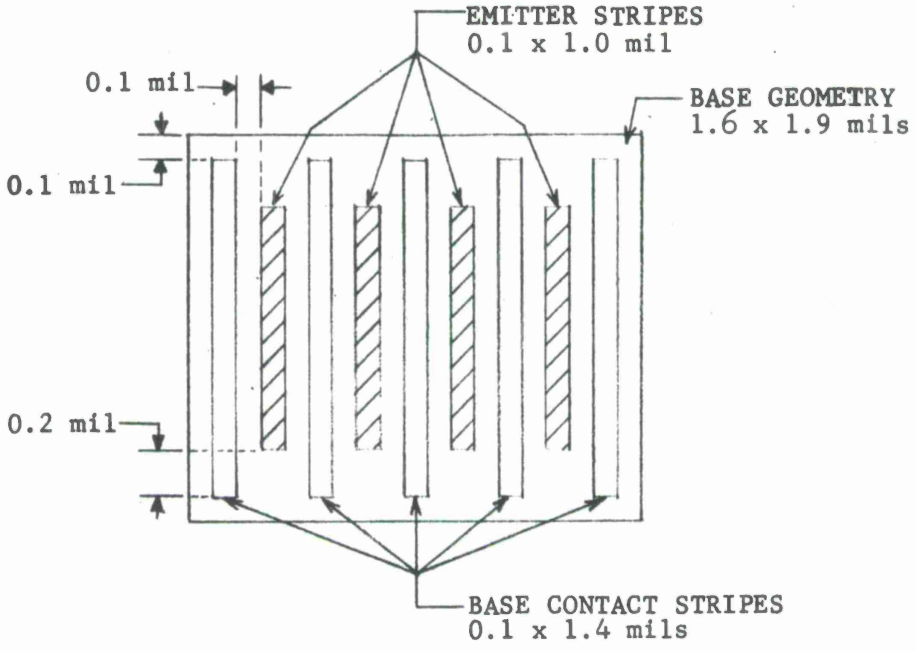
SECTION 2 - FACTUAL DATA

2.1 Development of High Speed Transistors

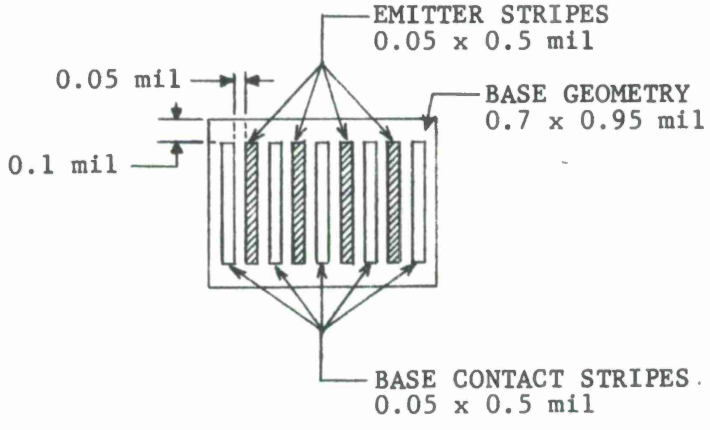
Because of the importance of transistor performance to the over-all speed properties of high speed microcircuits, a transistor development effort was conducted as part of this program. The basic principles of high performance design and fabrication, developed in part during an earlier phase of the program, were further developed to achieve transistors with higher speed and higher performance.

Most of the transistor development involved the use of 0.1-mil geometry, npn discrete (bottomside collector contact) and microcircuit (top collector contact) transistors; however, 0.05-mil geometry npn discrete transistors were also successfully fabricated utilizing similar high performance techniques. Figures 1a and 1b show the 0.1-mil and 0.05-mil geometry, respectively, of these discrete transistors.

Wafers of transistors were also fabricated for the purpose of studying those factors which affect parameter uniformity and yield in devices having high performance and small geometry. The findings of this effort resulted in significant improvements in the areas of photomask fabrication, photoengraving and metalization; these improvements are essential to the successful fabrication of



a. SX3



b. SX4

Figure 1. Transistor geometries.

high speed microcircuits of greater complexity, and in particular to the fabrication of complex high speed microcircuit arrays.

2.1.1 Transistors With 0.1-mil Geometry

During the past year, we have repeatedly demonstrated that high speed, 0.1-mil geometry npn transistors can be fabricated in discrete form and in monolithic microcircuits by using shallow diffusion techniques. Table 1 lists typical f_T properties of various 0.1-mil geometry structures that were fabricated. The data in Table 1 support the significant fact that high performance transistor designs can be incorporated into monolithic microcircuits even though the integrated circuit process adds fabrication complexity.

For high performance saturated switching applications, it is important for the transistors to have optimum f_T, r_b' and τ_s properties. Utilizing the fabrication techniques indicated above, including gold doping to minimize minority carrier lifetime, discrete transistors of the SX3 geometry (wafer 227A) were fabricated which exhibited f_T values as high as 6.5 GHz with r_b', τ_s and punchthrough voltage (V_{CES}) values of 17 Ω, 4-5 ns and 5.0 V, respectively. By varying the concentration of base impurities and the base width it was possible to make various compromises between f_T and V_{CES}. Table 2 lists typical parameter values for devices from wafers 229B and 235A, both of which had base impurity concentrations different than wafer 227A. Wafer 229B was more

TABLE 1

TYPICAL 0.1-MIL GEOMETRY TRANSISTOR PERFORMANCE

DEVICE	EMITTER GEOMETRY NO. & SIZE OF EMITTER STRIPES	BASE CONTACT GEOMETRY NO.& SIZE OF BASE CONTACT STRIPES	PEAK f_T (GHz)	I_C @ PEAK f_T (mA)
SMX1-T*	(2) - 0.1 x 1.5 mil	(3) - 0.1 x 1.5 mil	2.5 - 3.0	10 - 12
SMX2-T*	(1) - 0.1 x 0.8 mil	(2) - 0.1 x 0.8 mil	2.6 - 3.0	1.5 - 2.5
SMX3-T*	(2) - 0.1 x 1.5 mil	(3) - 0.1 x 1.5 mil	3.0 - 3.5	10 - 15
SMX4-TA*	(2) - 0.1 x 1.0 mil	(2) - 0.1 x 1.0 mil	2.8 - 3.5	10 - 13
SMX4-TB*	(3) - 0.1 x 1.3 mil	(3) - 0.1 x 1.3 mil	2.8 - 3.5	17 - 20
SX3**	(4) - 0.1 x 1.0 mil	(5) - 0.1 x 1.4 mil	3.0 - 6.0***	15 - 20

*Microcircuit transistor

**Discrete transistor

***The upper limit on f_T shown for the SX3 reflects the results of special fabrication techniques which had not yet been incorporated into the Integrated Circuit process.

TABLE 2

TYPICAL CHARACTERISTICS FOR TRANSISTORS WITH DIFFERENT BASE AND BASEWIDTH STRUCTURES

PARAMETER	TEST CONDITIONS	WAFER 229B	WAFER 235A
f_T	f_O = 300 MHz V_{CB} = 3 V	4.4 GHz	6.0 GHz
τ_s	$I_C = I_{B1} = I_{B2}$ = 8 mA	3.6 ns	3.7 ns
r'_b	I_C = 8 mA, I_{B1} = 3 mA	14.5 Ω	15.5 Ω
V_{CES}	I_E = 1 μA	7.0 V	3.0 V
h_{FE}	V_{CE} = 1 V, I_C = 0.1 mA	125	150

heavily doped, whereas 235A was less heavily doped than 227A. Devices from 235A also had narrower base widths.

It is important to note the relative independence of r_b' and τ_s to changes in base impurity structure in these shallow-diffused devices, in contrast with more conventional structures.

2.1.2 Transistors With 0.05-mil Geometry

During the 7th quarter of the program, the first 0.05-mil geometry (SX4) transistors were successfully fabricated. Typical devices exhibited peak f_T values of 6 GHz at collector currents of 4 to 5 mA, approximately 1/4 to 1/3 the peak f_T collector currents exhibited by SX3 (0.1-mil geometry) transistors with comparable impurity profiles and performance. See Figure 2. Earlier attempts at fabricating the SX4 were unsuccessful largely due to the need for improved techniques in photomask preparation.

Continued development of the SX4 geometry during the program extension is expected to provide additional information on the degree of improvement of transistor and microcircuit performance that can be obtained with the high performance diffusion techniques, by reducing device geometries as much as the state of the art will permit. It is anticipated that this type of device will be vital to the realization of very low power, very high speed, high density microcircuits.

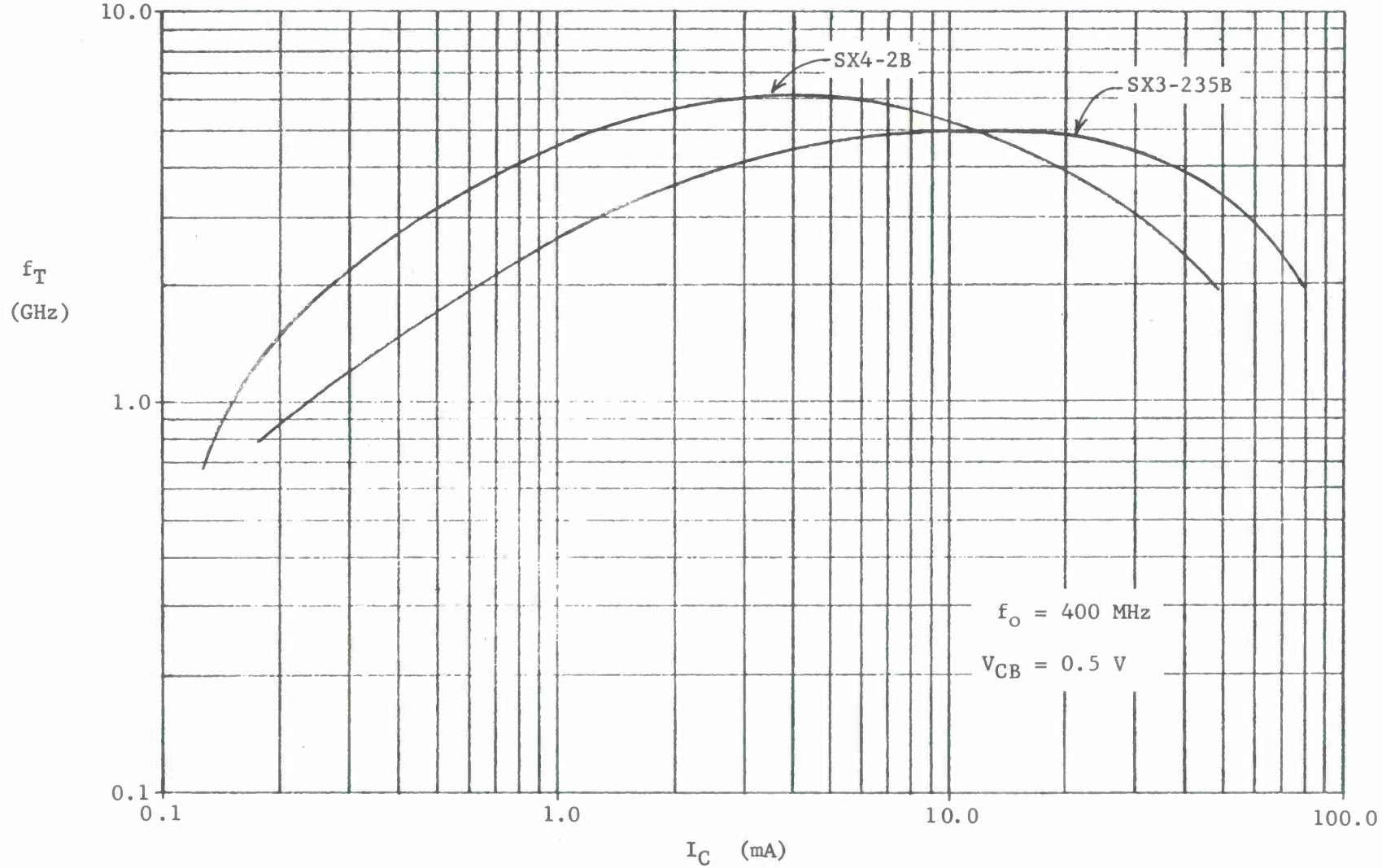


Figure 2. f_T vs. I_C characteristics for SX3 and SX4 geometries.

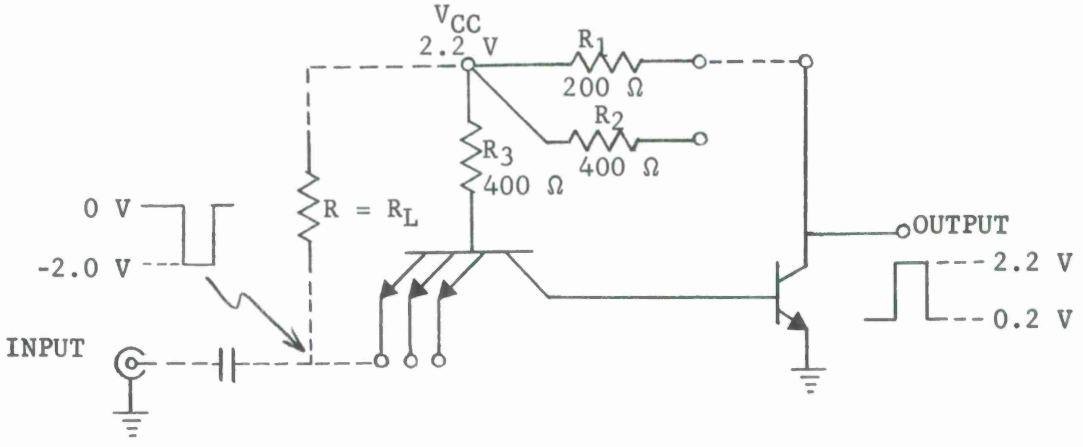
2.2 Development of High Speed Microcircuits

Microcircuit development, aimed at achieving subnanosecond circuit performance, has been performed using both saturating and non-saturating circuits. By incorporating high speed, small geometry transistors into equivalently small microcircuit structures, TTL (saturating) and ECL (non-saturating) 3-input gates have been fabricated which exhibit the lowest average propagation delay times that are known. The TTL microcircuit has demonstrated propagation delays of 1.3 ns/stage, whereas ECL gates have performed with propagation delays as low as 0.4 ns/stage.

2.2.1 Saturated Microcircuits - TTL

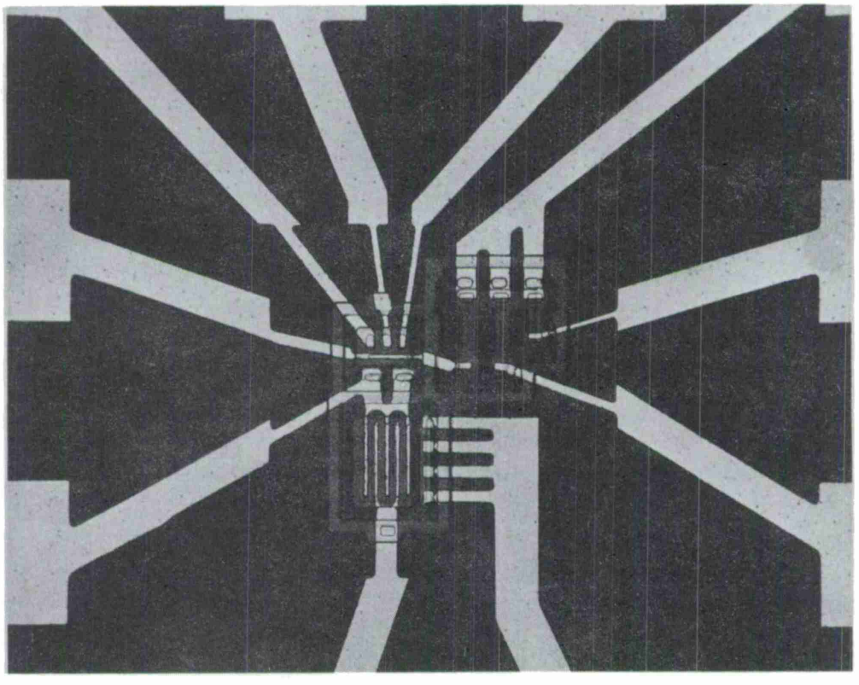
The saturated microcircuit developed on this program is the simple 3-input TTL gate shown schematically and topographically in Figure 3. This microcircuit, designated SMX1, with diffused regions occupying a total area of 20 square mils, was designed with an inverter transistor having an emitter with a multiple of 0.1-mil stripes, resistors of 0.3-mil geometry, and an equivalently small, multiple emitter gating element.

SMX1 microcircuits, fabricated with transistors having f_T values of 2.5 to 3.0 GHz, were shown to have propagation delay times as low as 1.3 ns at average power dissipations of 17 to 20 mW. Analyses indicated that this microcircuit design could have been further improved most effectively by optimizing the storage time



R_L = R_1, R_2 or the parallel combination of R_1 and R_2.

a. Schematic diagram.



b. Photomicrograph (M = 240X).

Figure 3. SMX1 Microcircuit.

properties (storage time contributes about 50% of the total propagation delay) of the inverter transistor. An increase in the transistor f_T without a reduction in storage time would have made only marginal improvements.

Several methods for reducing storage time without redesigning the microcircuit topography were considered. One method, which was unsuccessful, involved replacing the n+ buried collector regions by n+ epitaxial layers in an effort to reduce storage time through substrate transistor action. However, the basewidth of the substrate transistor (effectively the epitaxial layer thickness) was too great to permit proper substrate transistor action. In addition, removal of the buried n+ layer resulted in a factor of 3 increase in the normal 0.25 to 0.30 V transistor $V_{CE(SAT)}$ (measured at I_C = 10 mA, I_B = 1 mA). To effectively use substrate transistor action for reducing storage time would have required a redesign of the microcircuit. Only by redesigning the geometric configuration of the inverter transistor could the compromises in collector structure be worked out to provide effective substrate transistor action and low collector series resistance.

Speed-power properties of a number of SMX1 devices were examined to determine the relative utility of the basic TTL switching circuit in high-speed microcircuit systems and, in

particular, to determine its utility in high speed microcircuit arrays. A typical experiment run was one in which speed and power dissipation were monitored as R_L was varied in the microcircuit. The results are shown in Table 3. (Note the increased t_{off} time as R_L is increased. This increase is attributable to an increased parasitic $R_L C_{isol}$ time constant at the output node.) In another experiment where V_{CC} was varied and R_L kept constant at 180 Ω, propagation delays of 1.8 ns were obtained at power dissipations as low as 11.5 mW. These and other data taken on single SMX1 circuits and on a 5-stage SMX1 ring oscillator indicated that, based on present SMX1 performance levels, saturating microcircuits could be made which would function at average propagation delay times of 1 to 2 ns/stage at power levels of 8 to 12 mW/stage. The development of more effective means for reducing storage time can be expected to substantially improve this performance.

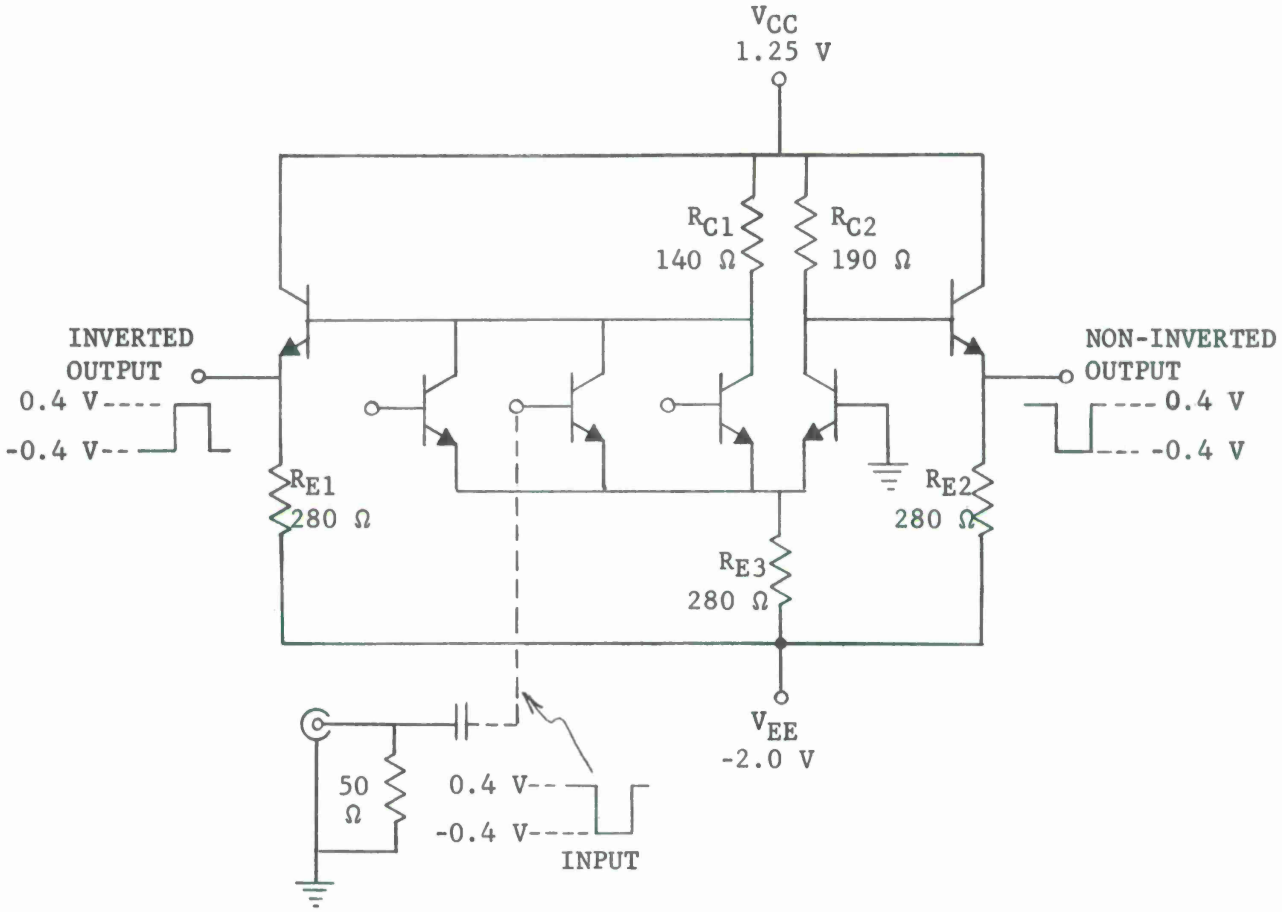
2.2.2 Non-saturating Microcircuits - ECL

The two ECL microcircuits evaluated in this part of the program were simple 3-input, complementary-output gates. The first, shown schematically and topographically in Figure 4, and designated the SMX2, was capable of operating at speeds as low as 0.4 ns with a total power dissipation (including both outputs) of 60 mW. The second ECL microcircuit, shown in Figure 5 and designated

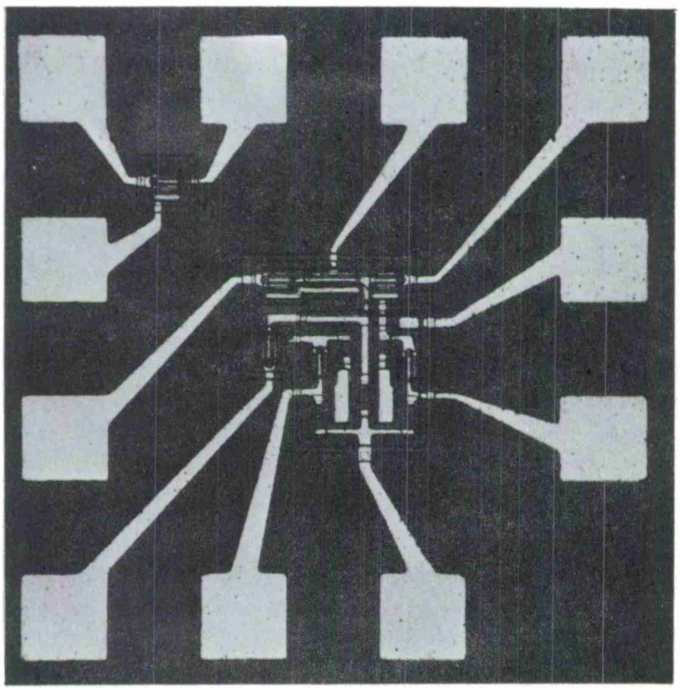
TABLE 3

SPEED-POWER DATA: SMX1, WAFER 28A

Collector Load Resistance	Typical t_{on} (ns)	Typical t_{off} (ns)	Average t_{pd} (ns)	Average Power Dissipation at 50% Duty Cycle (mW)
180 Ω (R_1)	0.90	1.70	1.3	19
310 Ω (R_2)	0.87	2.25	1.55	14
≈ 114 Ω (R_1 & R_2 in Parallel)	1.05	1.55	1.3	25

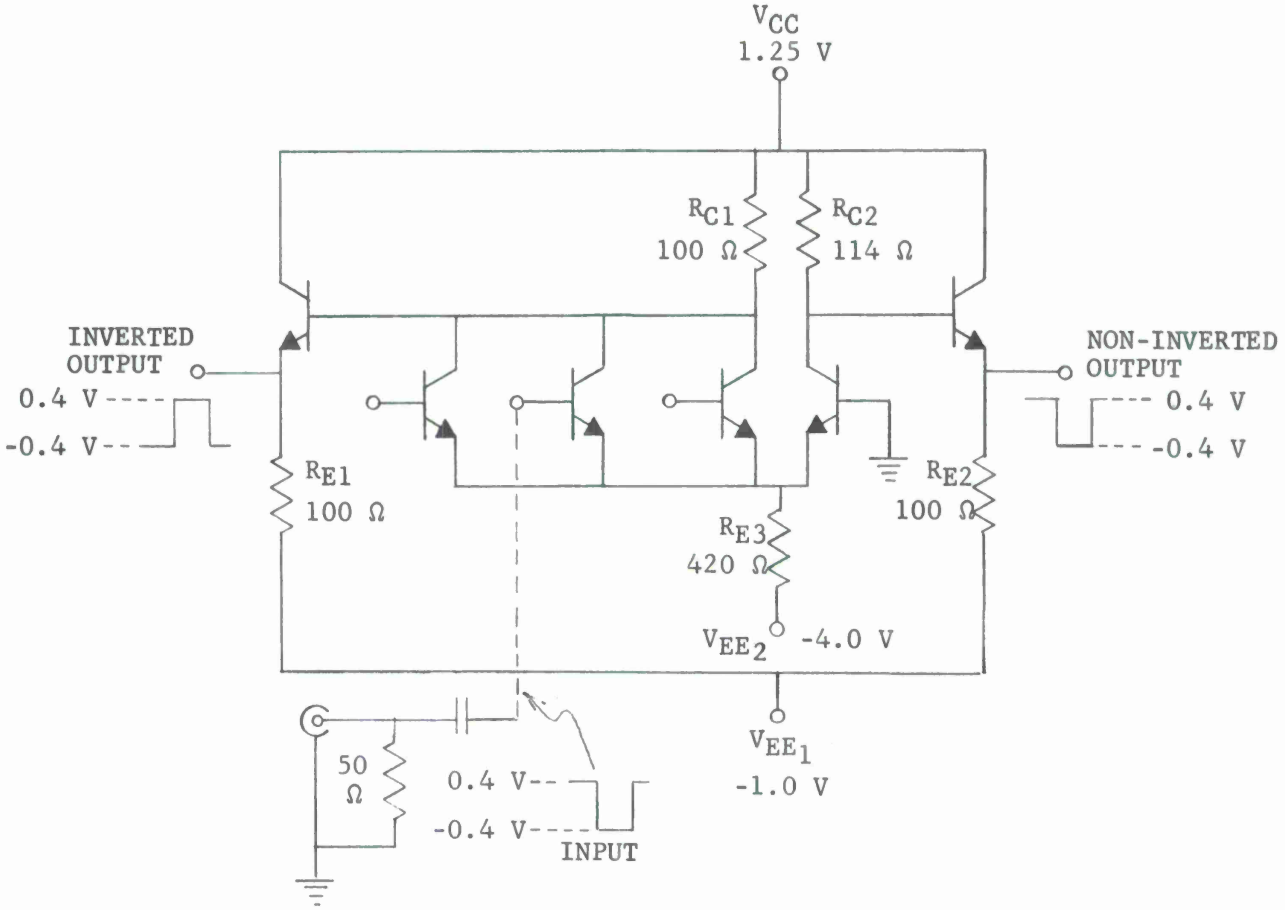


a. Schematic diagram.

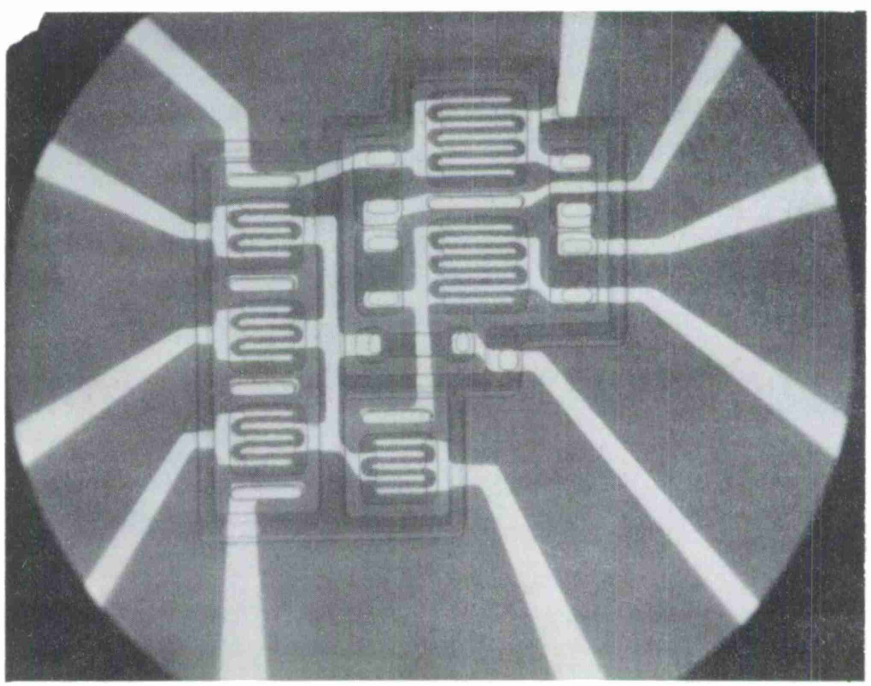


b. Photomicrograph (M = 150X).

Figure 4. SMX2 Microcircuit.



a. Schematic diagram.



b. Photomicrograph (M = 300X).

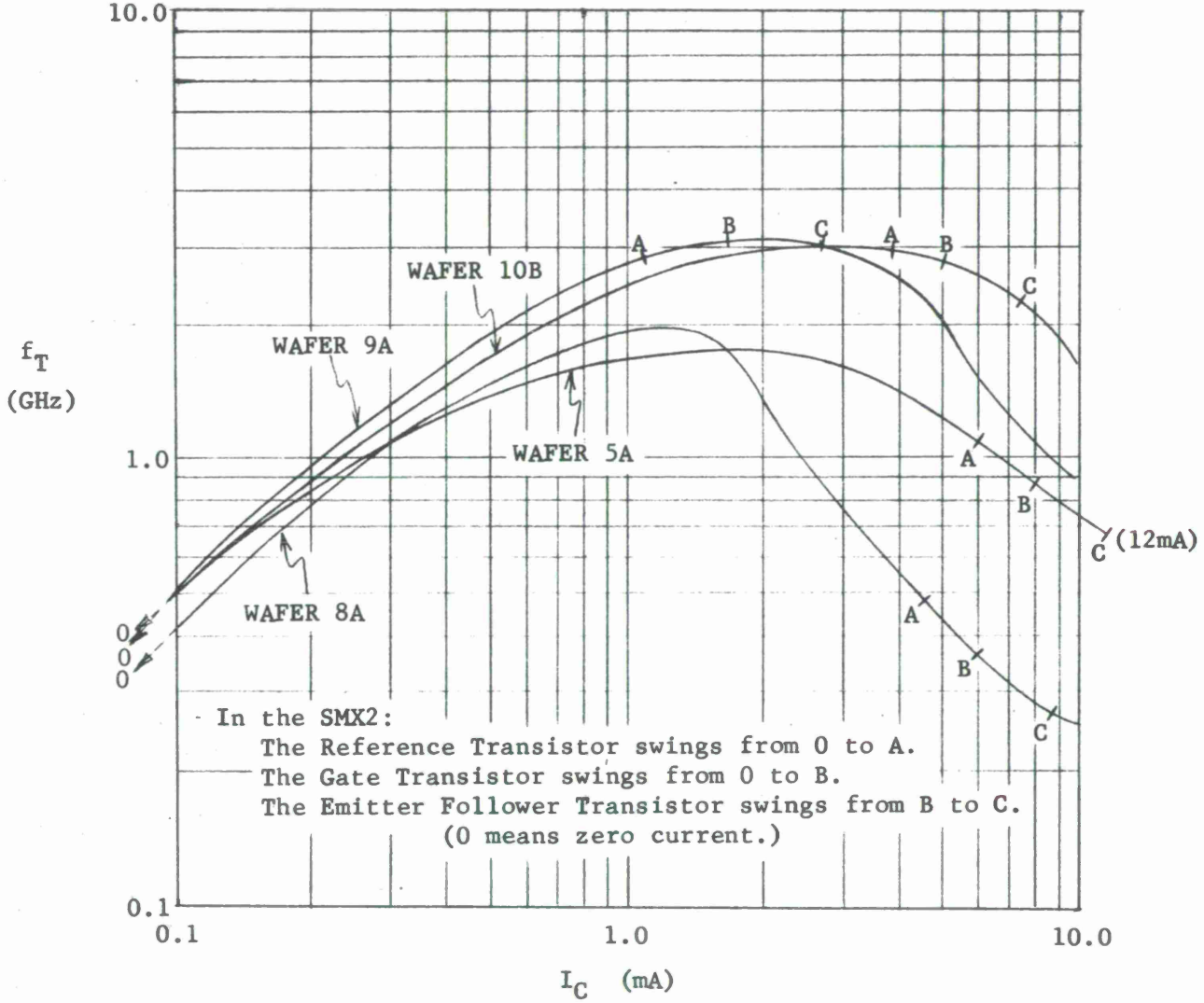
Figure 5. SMX4 Microcircuit.

SMX4 was designed to operate in the low tenth nanosecond range at slightly higher dissipations (80mW).

2.2.2.1 SMX2 Microcircuit

The first groups of SMX2 microcircuits that were fabricated had measured propagation delay times of 0.6 to 1.0 ns; however, analyses of data taken on these devices and on test transistors from the same wafers indicated that the basic SMX2 design should have been capable of better operating speeds. Specifically, circuit speed was being limited by (1) the maximum f_T of the microcircuit transistor and (2) the fact that the transistors were not biased to operate at currents at which f_T was optimum. By making appropriate changes in the transistor impurity structure and by adjusting resistor values it was possible to minimize these limitations to the extent that propagation delay times as low as 0.4 ns were obtained.

The basic dependence of the SMX2 on transistor performance is indicated by Figure 6. Displayed there are the f_T vs. I_C curves for representative transistors from four groups of SMX2 microcircuits, and the current operating ranges of the various circuit transistors. Included also is a table listing the measured speeds and load resistor values of the various groups of microcircuits. Figure 6 shows that in microcircuits from wafers 5A and 8A (slower microcircuits made early in the program), circuit transistors



AVERAGE PROPAGATION DELAY TIMES FOR VARIOUS SMX2 MICROCIRCUITS

Wafer No.	τ_{pd} (ns)	R_{E1}, R_{E2}, R_{E3} (ohms)
5A	0.6	210
8A	1.0	330
9A	0.6	800
10B	0.4	320

Figure 6. f_T vs. I_C characteristics for the transistors of the microcircuits listed in the table at right.

operated well out of their optimum speed range; the output transistors were operating far into the high current density regions (B-C) where f_T drops off and the average f_T of gate and reference transistors throughout their operating regions (0 to A and 0 to B, respectively) was also low. In microcircuits from wafer 10B, the peak f_T and f_T range were both increased, while maintaining the same current operating points. These improvements lowered the average propagation delay of the SMX2 to 0.4 ns.

Figure 6 also illustrates the relative effect of parasitic RC delays on SMX2 performance. In an attempt to optimize the speed-power characteristics in the microcircuits from wafer 9A, resistors were increased a factor of 2½ times the design value. A comparison of the speeds of devices from wafers 5A and 9A indicates that the consequent 2½-times increase in circuit parasitic RC delays in wafer 9A offsets the increase in speed that is expected from the improved transistor performance in 9A compared to 5A.

The speed-power performance of wafer 9A microcircuits was equally significant. It showed that simple 3-input, complementary-output ECL gates were capable of 0.6 ns operation at power dissipation of 18 to 19 mW. The equivalent dissipation for a single output gate would be 11 to 12 mW. Comparing this performance to the TTL it can be said that ECL gates can be made to operate at

power levels equivalent to TTL but with speeds 2 to 3 times faster.

2.2.2.2 SMX4 Microcircuit

Largely based on SMX2 microcircuit results, another ECL microcircuit, the SMX4, was designed. This microcircuit was intended to operate at low tenth nanosecond speeds. The basic approach to designing for the lower speed included (1) reducing circuit impedances to minimize RC delays; (2) redesigning the circuit transistors to operate at optimum speeds at the higher current levels and (3) minimizing unwanted charging delays at the gate emitter node by increasing R_{E2} to make this node appear as a constant current source. The circuit and microcircuit designs that resulted are shown in Figure 5.

Only one group of SMX4 circuits has been evaluated thus far. Average propagation delay for these devices was 0.7 ns. Analyses of the test results indicated that it may be possible to attain the intended 0.1 to 0.2 ns performance with this microcircuit design, but only if transistors with peak f_T values substantially higher than 3 GHz are used. The reasons for the failure of SMX4 microcircuits from wafer 2C to operate at low tenth nanosecond speeds are illustrated (see Figure 7) by comparing the f_T characteristics and circuit operating currents of SMX4 transistors from wafer 2C (τ_{pd} = 0.7 ns) with those of SMX2 transistors from wafer 10B (τ_{pd} = 0.4 ns). (Note that the SMX2 microcircuit uses one transistor design for gate, reference and output functions,

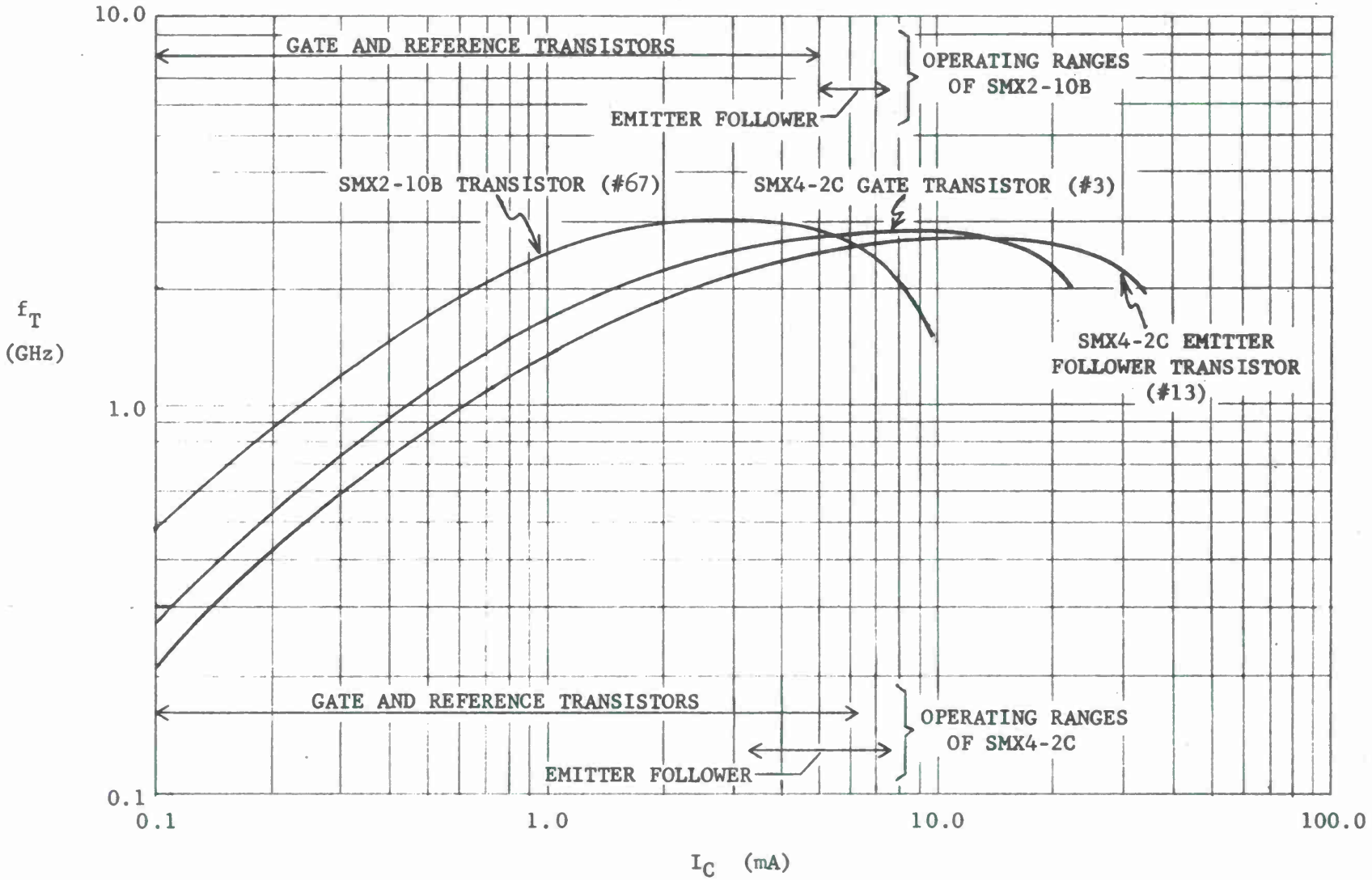


Figure 7. Curves of f_T vs. I_C, and operating ranges for SMX-10B and SMX4-2C transistors.

whereas the SMX4 utilizes one design for gate and reference transistors and another design for the output transistor.) It is seen that while devices from both microcircuits have similar peak values of f_T, the f_T values of the gating and reference transistors of the SMX2 are substantially higher than those of the SMX4 throughout their operating range; this occurs essentially because of the higher emitter transition capacitance of the larger SMX4 transistors. Only by increasing the transistor f_T throughout the operating range (equivalent to increasing peak f_T unless geometry is changed), is it possible that lower values of T_{pd} will be obtained.

Another group of microcircuits which we expect to have transistors with higher values of peak f_T than those of the SMX4-2C wafer are in preliminary stages of evaluation. Results of this evaluation will determine whether a redesign of the SMX4 will be necessary.

2.2.3 Parity Circuit Array

As stated previously, an important program goal during the last two quarterly periods has been to make a preliminary investigation of the speed improvements that are obtainable in digital systems through the fabrication and interconnection of many very high speed monolithic circuits within a single chip. Included in the effort has been the development of new techniques in fabrication,

interconnection and test required for the successful utilization of what is commonly referred to as the array technique.

The test vehicles selected for this investigation are 3-bit, 9-bit, and 27-bit versions of a complex computer circuit termed "Parity Check Circuit".

Much of the contract effort during the 7th quarter was devoted to determining the logic form and the microcircuit layouts for the high density, high speed parity circuit arrays. The effort included analysis of previously made microcircuits and transistors; a paper design of the high speed, low power ECL gate to be used in the array; discrete component breadboard study of the circuit design; and multilevel interconnection studies. Based on the results of this effort, the following decisions were made concerning the parity circuit arrays:

1. The logic form to be used is ECL.
2. The basic logic gate to be used is the 3-input, 1-output gate shown in Figure 8 and designated SMX5. A 5-stage ring oscillator constructed from microcircuit transistors similar to those to be used in the parity microcircuit, yielded average propagation delay times of 0.7 ns/stage at power levels which predict a total dissipation of 35 to 75 mW for the 3-bit parity circuit. The microcircuit arrays themselves are expected to operate at somewhat higher speeds.

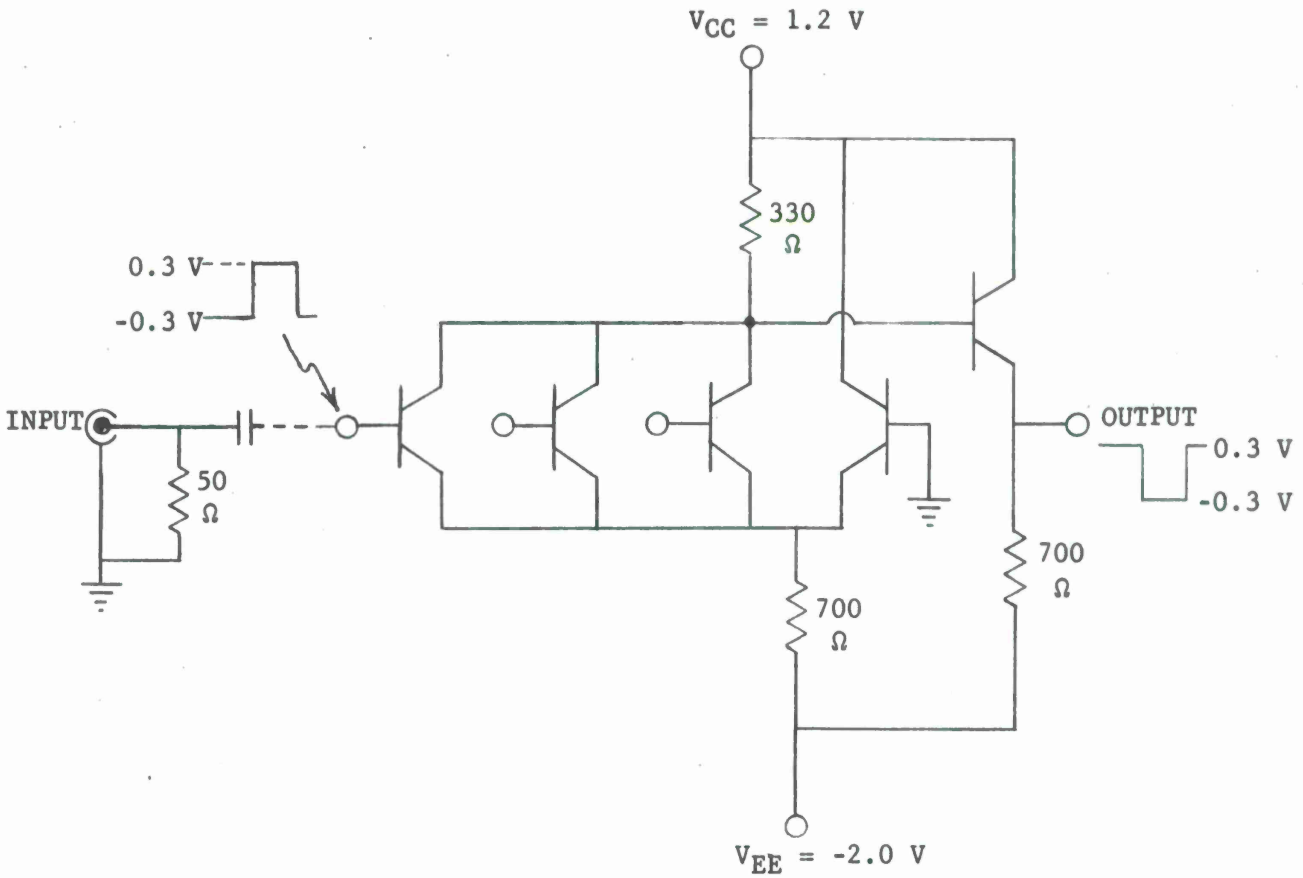


Figure 8. 3-input gate for parity array (SMX5).

3. Parity circuit array chips of 3, 9, and 27 bits are to be fabricated containing 58, 232 and 754 components, respectively. It is intended to fabricate the 3-bit parity circuit as a repeated cell on the wafer and to generate through multilevel interconnecting the 9- and 27-bit arrays on a single silicon chip. Figure 9 is the schematic diagram for the 3-bit circuit. Figure 10 is the functional diagram of the 27-bit array, composed of thirteen 3-bit circuits.

4. The multilevel interconnection system to be used will utilize aluminum conductor layers and vapor-deposited SiO_2 insulator layers.

By the end of the 7th quarter, preliminary design of the masks and layout for the three parity circuits had commenced.

A substantial program effort during the 8th quarterly period was directed toward completion of the microcircuit layout design for the three parity circuits, generation of the photomasks for the same, continued development of the multilevel metalization system, and commencement of fabrication of the 3-bit circuit.

By the end of the 8th quarterly period design work was completed on the 3-bit and 9-bit circuits, photomasks for the 3-bit circuit had been generated and fabrication of the 3-bit circuit was begun.

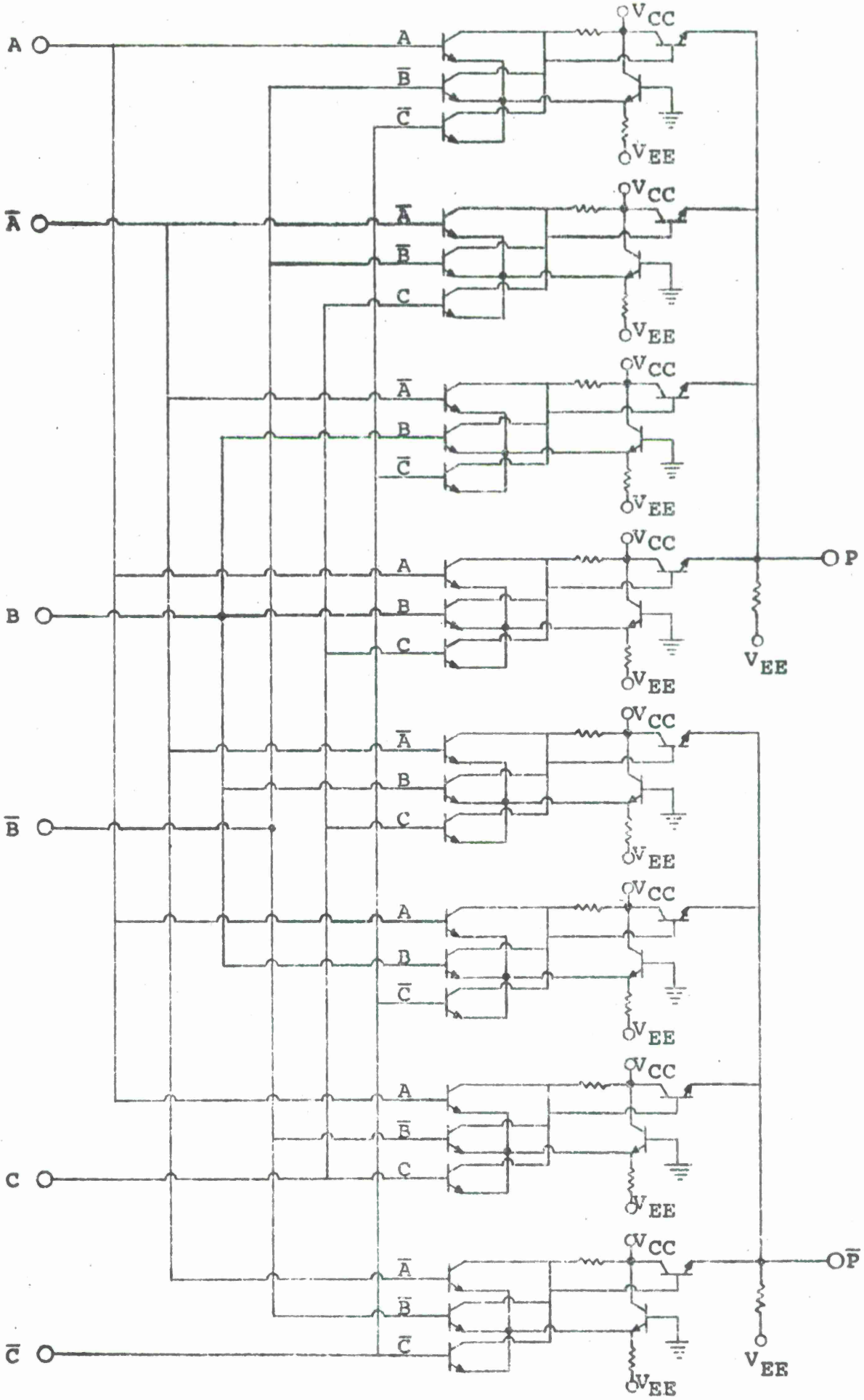


Figure 9. Schematic diagram of 3-bit parity circuit.

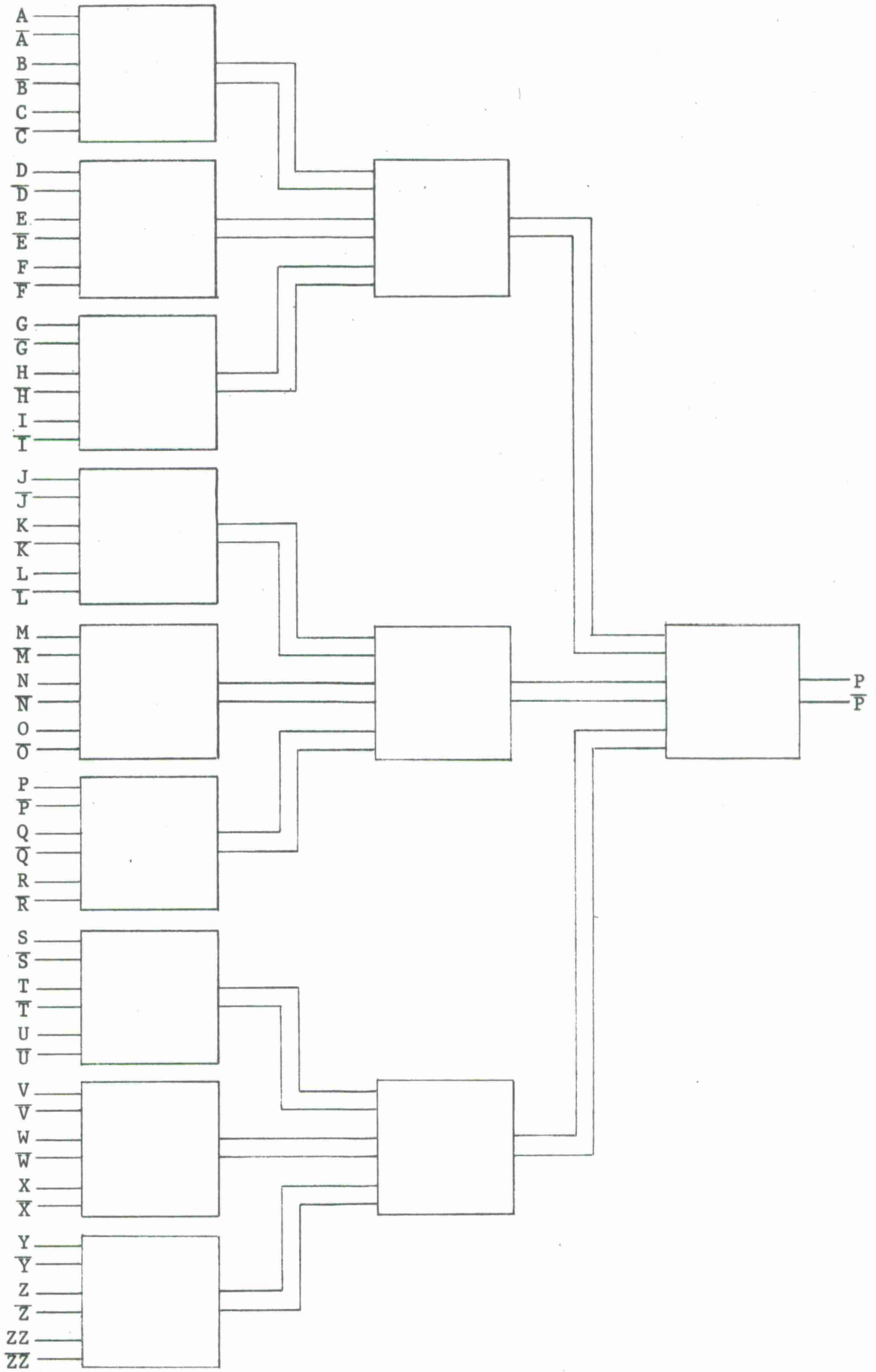


Figure 10. 27-Bit Parity Circuit.

According to the present plans, the 9-bit and 27-bit circuits will be fabricated using three levels of metalization; the 3-bit circuit will be fabricated with 2 and 3 levels of metalization. Chip sizes for the 3-, 9-, 27-bit arrays will be 30 x 34 mils, 45 x 51 mils and 85 x 90 mils, respectively.

Figure 11 is a photomicrograph of the 3-bit cell prior to metalization. The total area occupied by the cell is 14.7 x 14 mils.

It is expected that during the next quarterly period, the first 3-bit arrays will be available for evaluation. It is further expected that the design of the multilevel interconnection layouts for the 27-bit array will be completed and that the generation of the photomasks for the 9- and 27-bit circuits will also be completed.

2.2.4 Fabrication of Microcircuits for Computer Circuit Evaluation

The major approach of the microcircuit effort described in paragraph 2.2.3 was to study those factors in microcircuits which relate to high speed performance, and particularly to subnanosecond performance. The purpose of the microcircuit work described here is to study the speed improvements that can be made in an existing circuit design by fabricating it in microcircuit form, utilizing the high performance techniques developed in the other study.

Toward this end an ECL type circuit being used as part of an

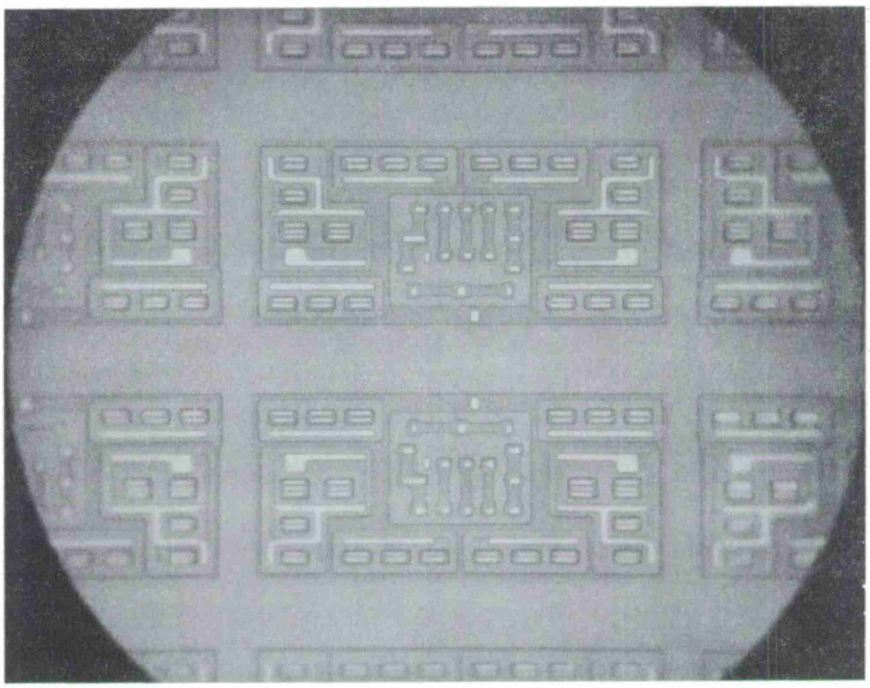


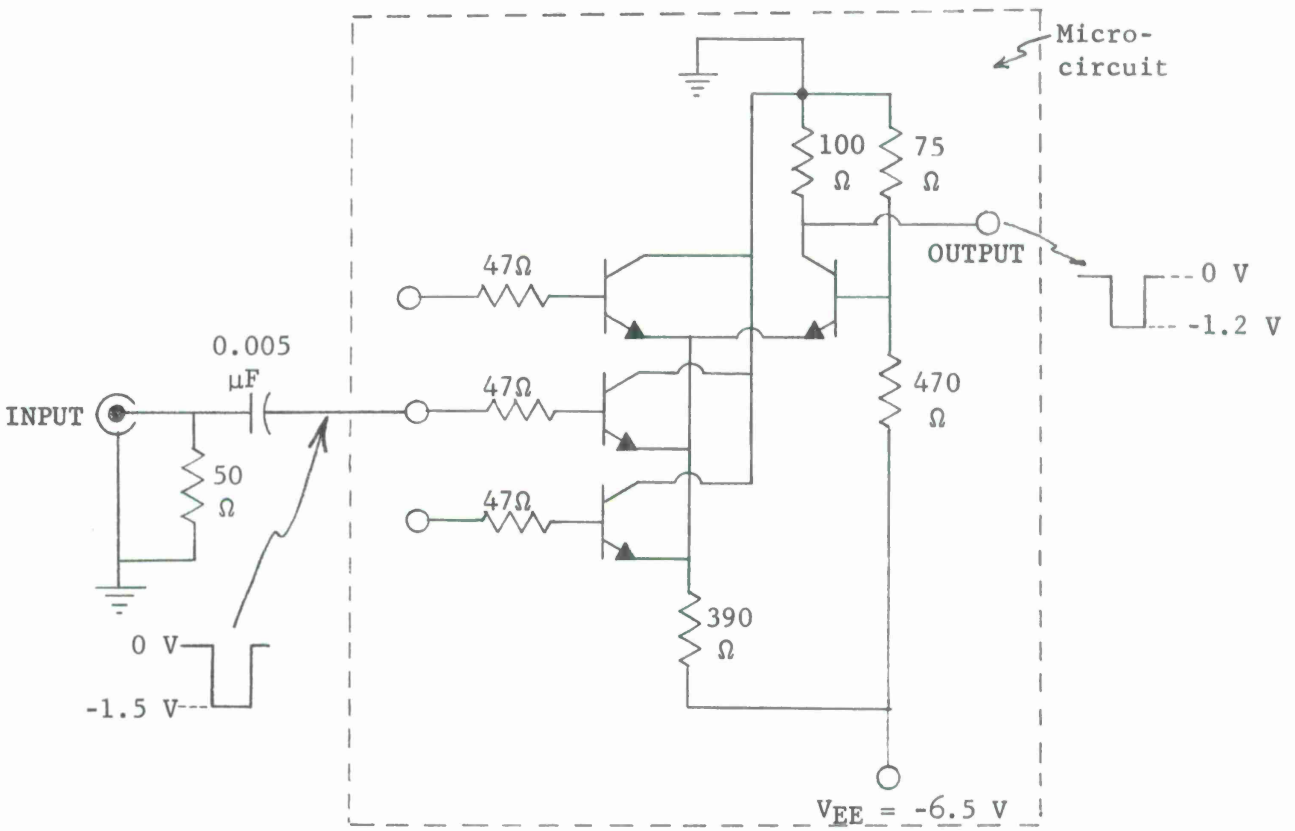
Figure 11. Photomicrograph of the 3-bit parity cell prior to metalization. (M = 150X)

experimental computer circuit design by Lincoln Laboratory, was designed and fabricated in microcircuit form. See Figure 12. Insertion of SX3 type transistors having f_T of 3 GHz into the breadboard circuit had reduced the circuit propagation times from 5.0 ns to 1.8 ns. Substantial additional improvements in speed are expected of the microcircuit.

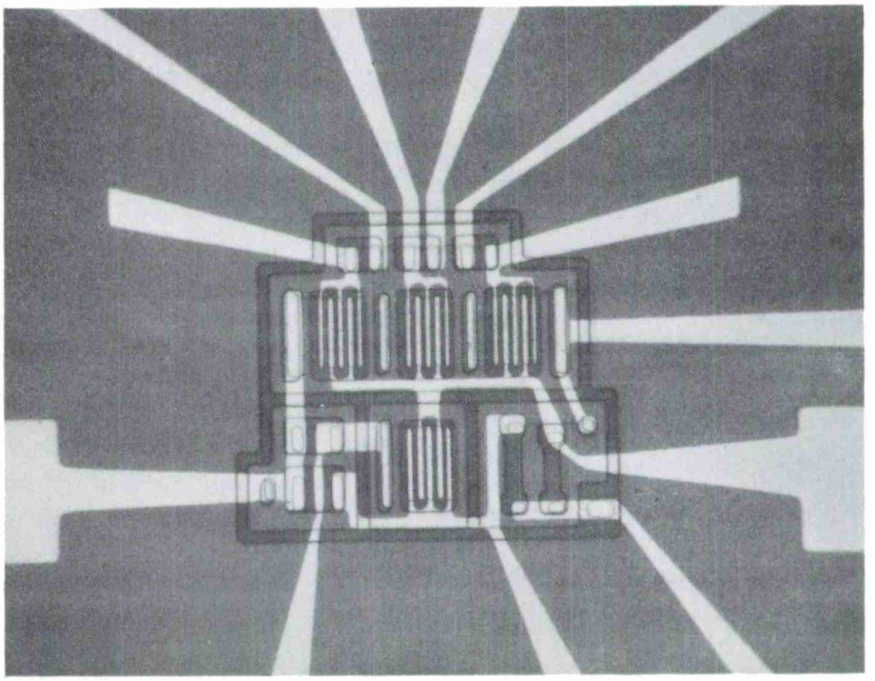
Several lots of SMX3 microcircuits containing transistors having f_T of 3 to 3.5 GHz were fabricated and tested. Measured propagation delay times of less than 1 ns were observed.

The first of the microcircuits fabricated (wafer 2B) had bias resistors lower than design value. At prescribed bias voltages these low value resistors caused excessive collector current to flow and resulted in saturation of the gating transistors, which in turn resulted in circuit propagation delay times in excess of 5 ns. The saturation was the result of excessive voltage drop due to the large currents flowing in the transistor collector resistance.

Subsequently fabricated SMX3 wafers (wafer 4A being typical) were made with resistors having larger values. They were also gold doped to provide minimum storage time in the event of saturation with the higher value resistors. Twenty microcircuits (all of which had τ_{pd} less than 1 ns) from wafer 4A were delivered to Lincoln Laboratory for evaluation. Table 4 gives the switching



a. Schematic diagram.



b. Photomicrograph (M = 220X).

Figure 12. SMX3 Microcircuit.

TABLE 4

A-C SWITCHING DATA FOR COMPUTER MICROCIRCUITS FROM WAFER SMX3-4A

UNIT	GATE INPUT TERMINAL NO.	t_{off} (ns)	t_{on} (ns)	t_{pd} (ns)	UNIT	GATE INPUT TERMINAL NO.	t_{off} (ns)	t_{on} (ns)	t_{pd} (ns)
AA012	3	1.10	0.82	0.96	AA023	3	0.95	0.82	0.89
	4	1.10	0.82	0.96		4	0.98	0.85	0.92
	5	1.06	0.91	0.99		5	0.93	0.82	0.88
AA016	3	0.85	0.84	0.85	AA026	3	0.94	0.75	0.85
	4	0.94	0.86	0.90		4	0.95	0.76	0.86
	5	0.91	0.83	0.87		5	0.96	0.78	0.87
AA017	3	1.04	0.95	1.00	AA027	3	1.23	0.64	0.94
	4	1.05	0.97	1.01		4	1.22	0.61	0.92
	5	0.95	0.97	0.96		5	1.18	0.59	0.89
AA019	3	0.93	0.80	0.87	AA028	3	0.90	0.73	0.82
	4	0.98	0.84	0.91		4	0.93	0.76	0.85
	5	0.92	0.81	0.87		5	0.94	0.77	0.86
AA020	3	1.03	0.74	0.89	AA029	3	1.15	0.69	0.92
	4	1.0	0.74	0.87		4	1.18	0.74	0.96
	5	1.0	0.75	0.88		5	1.08	0.70	0.89

data for a sampling of 10 of the devices.

The extent of the improvements in system speed that result from incorporation of these microcircuits in the computer system is not known at this time since the Lincoln Laboratory evaluations of the microcircuits have not been completed.

SECTION 3 - DELIVERIES OF SAMPLE DEVICES

During the past year the following packaged transistor and microcircuit samples were delivered to Lincoln Laboratory for evaluation:

Sample Category	Sample Type	Quantity
Discrete Transistors	SX3	39
	SX4*	2
Microcircuit Transistors	SMX2T	3
TTL Microcircuits	SMX1	19
ECL Microcircuits	SMX2	19**
	SMX3	22
	SMX4	5

*In additional to the two (2) packaged SX4 transistors, nine (9) unpackaged SX4 chips were delivered.

**This quantity includes the microcircuits used in the two 5-stage ring oscillators.

SECTION 4 - FUTURE WORK

Program effort during the next quarterly period will be directed toward:

1. Continued development of high speed, high performance transistor fabrication techniques.
2. Continued development of high speed microcircuits. Included will be an evaluation of the low tenth nanosecond capabilities of the SMX4. In particular it is to be determined if the gating and reference transistor geometries impose a speed limitation on the microcircuit and whether a redesign is necessary to achieve the desired 0.1 to 0.2 ns performance.
3. Fabrication of the 3-bit Parity Circuit Array.
4. Generation of the photomasks for 9-bit Parity Circuit Array and fabrication of the same.
5. Generation of the photomask for the 27-bit Parity Circuit Array.

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13. ABSTRACT

This Eighth Quarterly Summary Report describes the research and development program of the Philco Microelectronics Division, under subcontract to Lincoln Laboratory, M.I.T. In addition to presenting the work performed during the last quarter, the report summarizes earlier work.

The primary objective of this program was the fabrication of silicon monolithic microcircuits with average propagation delay times in the nanosecond region. Since this goal was achieved early, experiments were directed toward achieving subnanosecond microcircuits. A second objective has been the investigation of the technological problems of the fabrication of ultrahigh-speed complex bipolar arrays.

The report describes the following: (1) the development of 0.1- and 0.05-mil geometry high-speed transistors, (2) the development of saturated and unsaturated high-speed microcircuits, (3) the progress of the array investigation, using 3-, 9-, and 27-bit ECL versions of a parity generator as test vehicles, and (4) the design and fabrication of microcircuit form of an ECL type circuit which is being evaluated by Lincoln Laboratory as part of an experimental computer circuit design.

14. KEY WORDS

microelectronics
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high-speed transistors
high-speed microcircuits